REMARKS

A drawing correction for Figure 4 is submitted that replaces Figure 4 as filed. The change is consistent with the proposed drawing correction submitted on January 24, 2003 and approved by the Examiner.

Claims 1-14 were previously pending in the application. Claims 2 and 6 are cancelled, leaving claims 1, 3-5 and 7-14 for consideration.

Claims 1-3, 7 and 8 are rejected as being anticipated by POCHOLLE et al. 4,917,450.

Reconsideration and withdrawal of the rejection are respectfully requested because the reference does not disclose or suggest that one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line as recited in claim 1 of the present application.

The above recitation of a peer-to-peer connection was originally presented in claim 6 and is not disclosed by POCHOLLE et al. Specifically, column 2, lines 52-59, of POCHOLLE et al. disclose that photodiodes 5 to 8 receive emitted light and convert light into electrical signals representing binary data. The reception of light and conversion into electrical signals representing binary data as taught by POCHOLLE et al. is not a peer-to-peer connection and thus POCHOLLE et al. do not teach

that one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line as recited in claim 1 of the present application.

Claims 2, 3, 7 and 8 depend from claim 1 and further define the invention and are also believed patentable over POCHOLLE et al.

Claims 1-5 and 7 are rejected as anticipated by LEVI et al. 5,148,504.

Reconsideration and withdrawal of the rejection are respectfully requested because the reference does not disclose or suggest that one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line as recited in claim 1 of the present application.

Column 13, lines 11-31 of LEVI et al., for example, teach an optical-to-electrical conversion between integrated circuits 102 and 103 and unshown contacts made using guides 106. Such optical-to-electrical conversion using optical guides is not a peer-to-peer connection via at least one transmission line as recited in claim 1 of the present application. As the reference does not disclose that which is recited, the anticipation rejection is not viable. Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 2-5 and 7 depend from claim 1 and further define the invention and are also believed patentable over LEVI et al.

Claims 1, 6 and 13 are rejected as being anticipated by CARLSON et al. 5,506,961.

Reconsideration and withdrawal of the rejection are respectfully requested because the reference does not disclose or suggest that a plurality of processing elements are located around a single switcher as recited in claim 1 of the present application.

As seen in Figure 1 of CARLSON et al., for example, processing elements 120 are each connected by a single bus to central processing unit 105 (indicated in the Official Action as a single switcher). Accordingly, the plural processing elements are located to one side of the processor and are not plural processing elements that are located around a single switcher as recited in claim 1 of the present application.

In addition, the Official Action has offered elements 105 (central processing unit), 110 (primary memory) and 115 (system I/O bus) as a single switcher.

MPEP §2111 states that during patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification". *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969). The "PTO applies to verbiage of the proposed claim, the broadest

reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification."

One of ordinary skill in the art would understand a switcher to provide communication function between processors. The primary memory 110 and the bus line 115 do not perform this function. Accordingly, one of ordinary skill in the art would understand that these are separate elements that are distinct from a switcher or the central processing unit 105 of CARLSON et al.

Accordingly, CARLSON et al. disclose what is taught as prior art on page 3, lines 4-6 and page 6, lines 1-17 of the present application in conjunction with Figure 1 of the present application. Specifically, CARLSON et al. teach a number of chips arranged in a multi-chip module as processing elements that are connected via a common bus. Therefore, the broadest reasonable interpretation of one of ordinary skill in the art would not include each of elements 105, 110 and 115 as part of a single switcher.

Further, the broadest reasonable interpretation of "network interface" would be interpreted by one of ordinary skill in the art as the point of communication between the processing

elements and the switcher. A bus interface (noted in the Official Action as a network interface) would be an interface between the processing element and the bus line, not the processing element and the switcher. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

Claims 1-5 and 14 are rejected as anticipated by HARTMANN 6,018,782.

Reconsideration and withdrawal of the rejection are respectfully requested because the reference does not disclose or suggest that one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line as recited in claim 1 of the present application.

Column 6, lines 29-39 of HARTMANN disclose that communication is transferred from an input buffer 410 coupled to an inter-module link 230 to an output buffer 420 coupled to a second inter-module link 230. An associated address uniquely identifies a destination address for the data packet. A controller operates to determine a destination for the data packet and routes the data packet to the destination via an appropriate inter-module link 230.

The above-described communication is not a peer-to-peer connection via at least one transmission line as recited in claim

1 of the present application. As the reference does not disclose that which is recited, the anticipation rejection is not viable. Reconsideration and withdrawal of the rejection are respectfully requested.

Claim 14 is rejected as being anticipated by BERNET et al. 5,764,645.

Reconsideration and withdrawal of the rejection are respectfully requested because the reference does not disclose or suggest that one of the plurality of processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line as recited in claim 14 of the present application.

Column 1, lines 5-9, of BERNET et al. teach that the invention of BERNET et al. relates to ATM (asynchronous transfer mode) communication networks. Accordingly, the devices of BERNET et al. are connected by ATM connections and are not connected by peer-to-peer connection via at least one transmission line as recited in claim 14 of the present application.

Claims 1 and 9-12 are rejected as anticipated by YOSHIMURA et al. 6,343,171.

Reconsideration and withdrawal of the rejection are respectfully requested because the reference does not disclose or suggest that one of the plurality of processing elements and the single switcher are connected by peer-to-peer connection via at

least one transmission line as recited in claim 1 of the present application.

Column 56, lines 35-52 of YOSHIMURA et al. teach optical transmission of signals to other electro-optic devices in an interposer, multi-chip module, or inter-multi-chip package. Such optical transmission of signals is not a peer-to-peer connection via at least one transmission line as recited in claim 1 of the present application. As the reference does not disclose that which is recited, the anticipation rejection is not viable. Reconsideration and withdrawal of the rejection are respectfully requested.

Claim 14 is rejected as anticipated by MENDELSON et al. 6,343,083.

Reconsideration and withdrawal of the rejection are respectfully requested because the reference does not disclose or suggest that one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line as recited in claim 14 of the present application.

Column 1, lines 8-14, of MENDELSON et al. disclose that the invention of MENDELSON et al. relates to a connectionless protocol, such as IP over Ethernet, over a connection-oriented network, such as an ATM network. An asynchronous transfer mode connection is not a peer-to-peer connection via at least one

transmission line as recited in claim 14 of the present application. As the reference does not disclose that which is recited, the anticipation rejection is not viable. Reconsideration and withdrawal of the rejection are respectfully requested.

An object of the present invention is to simplify the connection between processing elements so that the processing elements and a switcher can be implemented in a single semiconductor chip and at least one of the processing elements and the switcher can be connected by peer-to-peer connection via at least one transmission line.

The only reference cited in the Official Action that teaches peer-to-peer communication is CARLSON et al. Specifically, column 6, lines 10-23, of CARLSON et al. teach peer-to-peer authorization from a system authorizer mechanism 112. The function of system authorizer mechanism 112 is to authorize whether a server connection manager should comply with an open request from a client connection manager. On page 4 of the Official Action, system authorizer mechanism 112 is combined with central processing unit 105, primary memory 110 and I/O bus line 115 as part of the single switcher. Accordingly, any proposed modification of a reference to include peer-to-peer communication as taught by CARSLON et al. must include each of elements 105, 110, 115 and 112. One of ordinary skill in the art

would not be motivated to include each of these elements because they would increase the size of the semiconductor chip, which goes against each of the teachings of the references of minimizing a chip size. Accordingly, based on the characterization of a switcher as offered in the Official Action, there would be no motivation to combine CARLSON et al. with any of the previously cited references to render obvious claims 1, 3-5 and 7-14 of the present application.

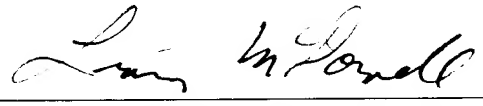
In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Should there be any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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APPENDIX:

The Appendix includes the following item:

- a Replacement Sheet for Figure 4 of the drawings